Fig.1(a)

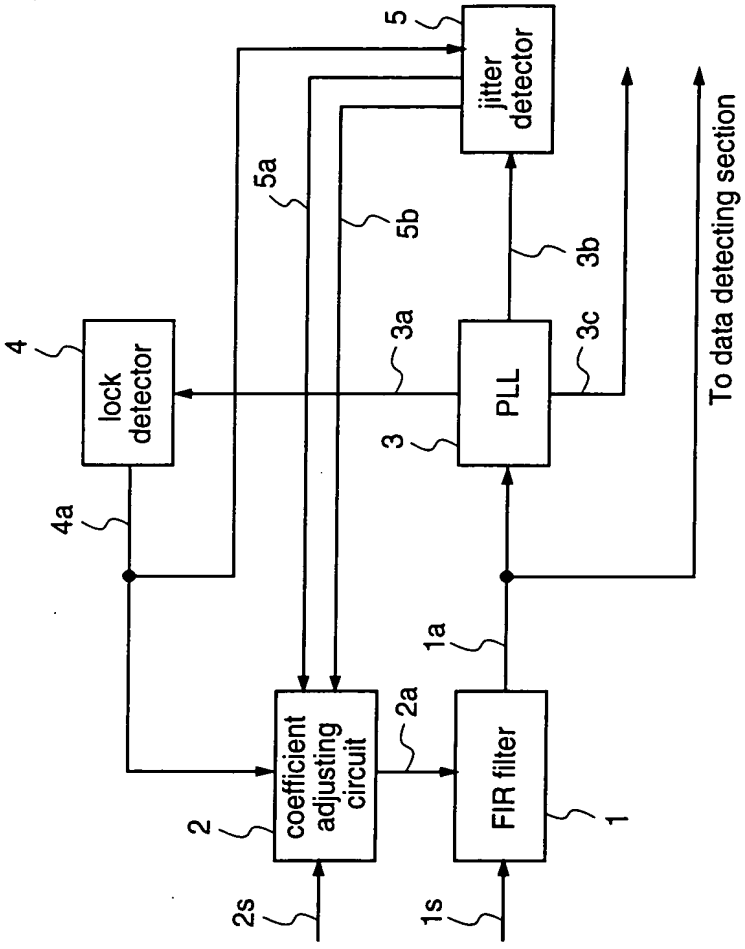

jitter detector
5
5a
5b
lock detector
4
4a
3a
PLL
3
3b
3c
To data detecting section
coefficient adjusting circuit
2
2a
FIR filter
1
1a
2s
1s

Fig.1(b)

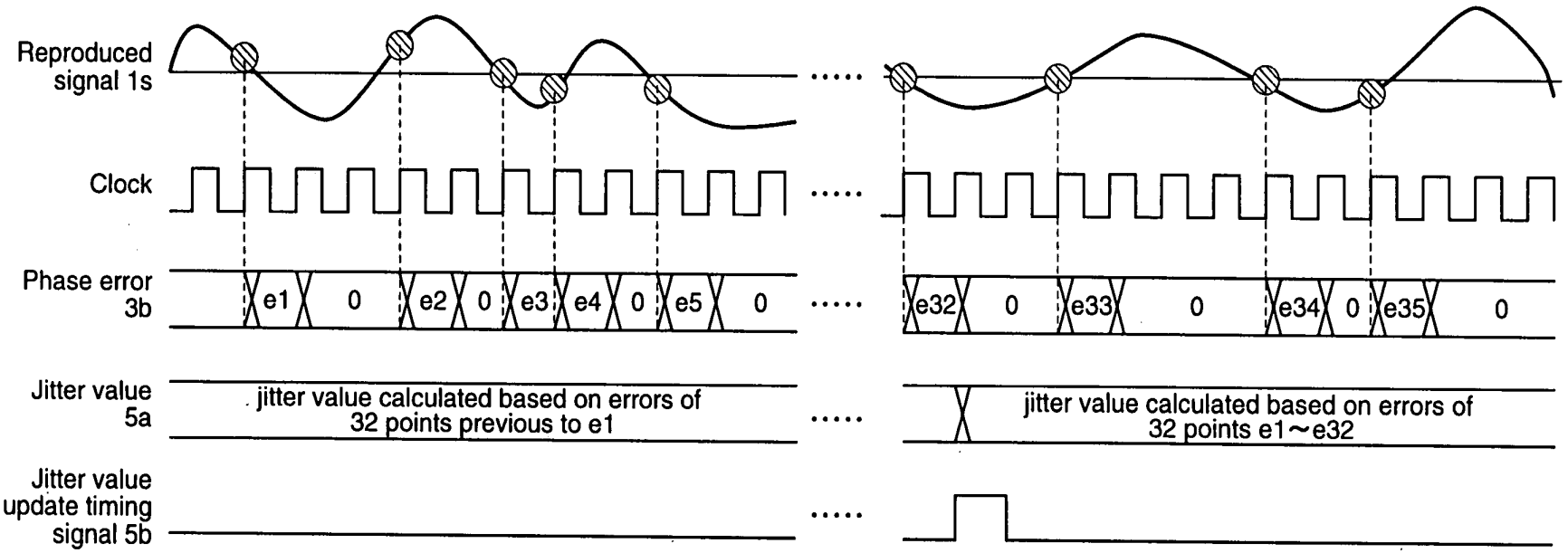

Reproduced signal 1s
Clock
Phase error 3b
e1
0
e2
0
e3
e4
0
e5
0
e32
0
e33
0
e34
0
e35
0
Jitter value 5a
jitter value calculated based on errors of 32 points previous to e1
jitter value calculated based on errors of 32 points e1～e32
Jitter value update timing signal 5b

Fig.2

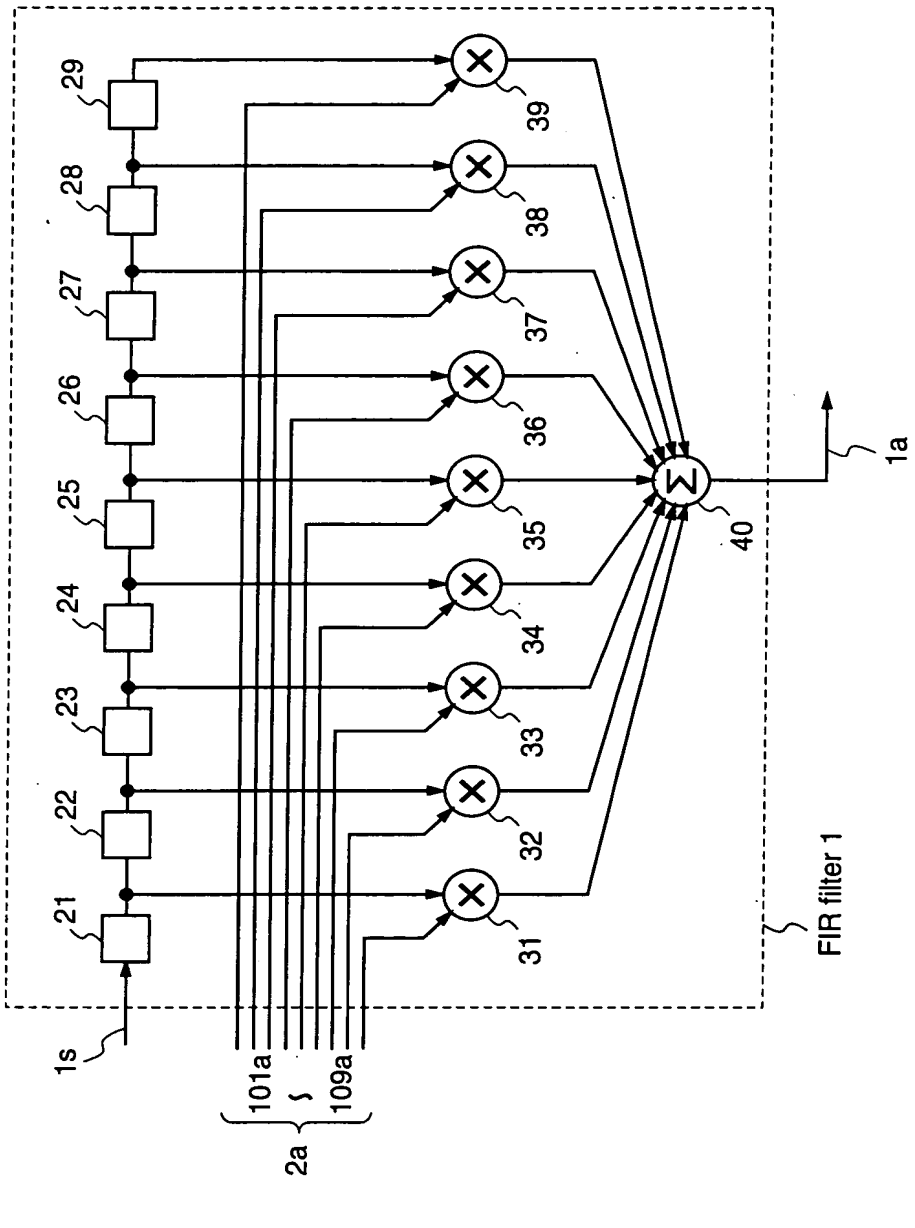

1s
21
22
23
24
25
26
27
28
29
31
32
33
34
35
36
37
38
39
40
Σ
1a
FIR filter 1
2a
101a
109a

Fig.3

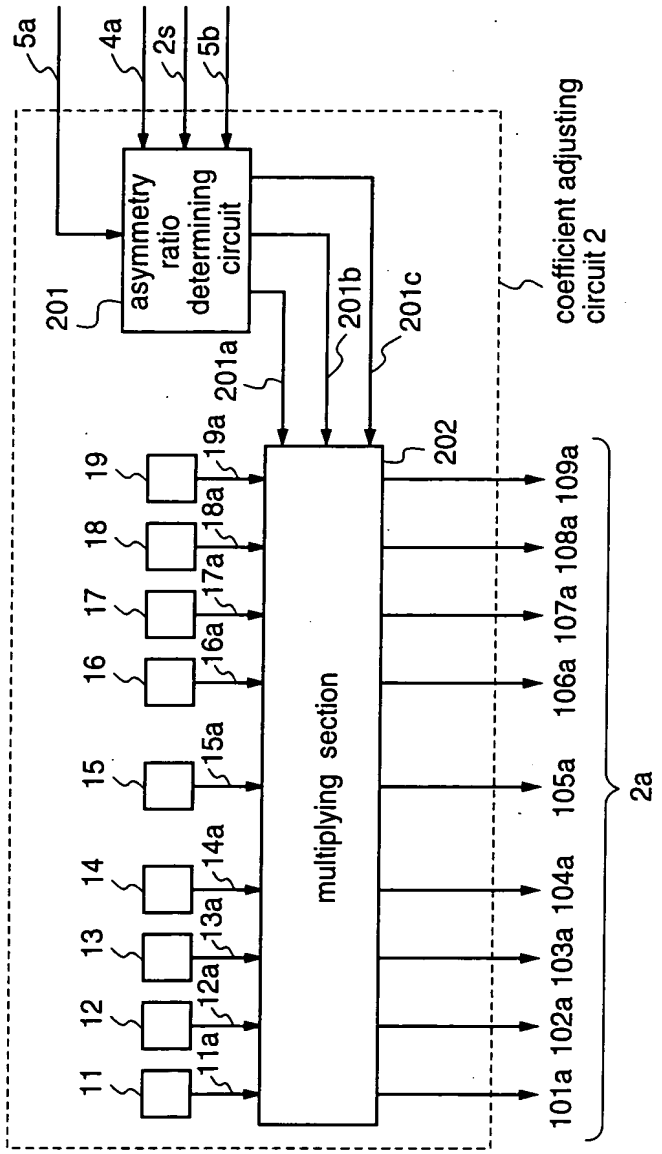

5a
4a
2s
5b
asymmetry ratio determining circuit
201
201a
201b
201c
202
coefficient adjusting circuit 2
multiplying section
11
12
13
14
15
16
17
18
19
11a
12a
13a
14a
15a
16a
17a
18a
19a
101a
102a
103a
104a
105a
106a
107a
108a
109a
2a

Fig.4

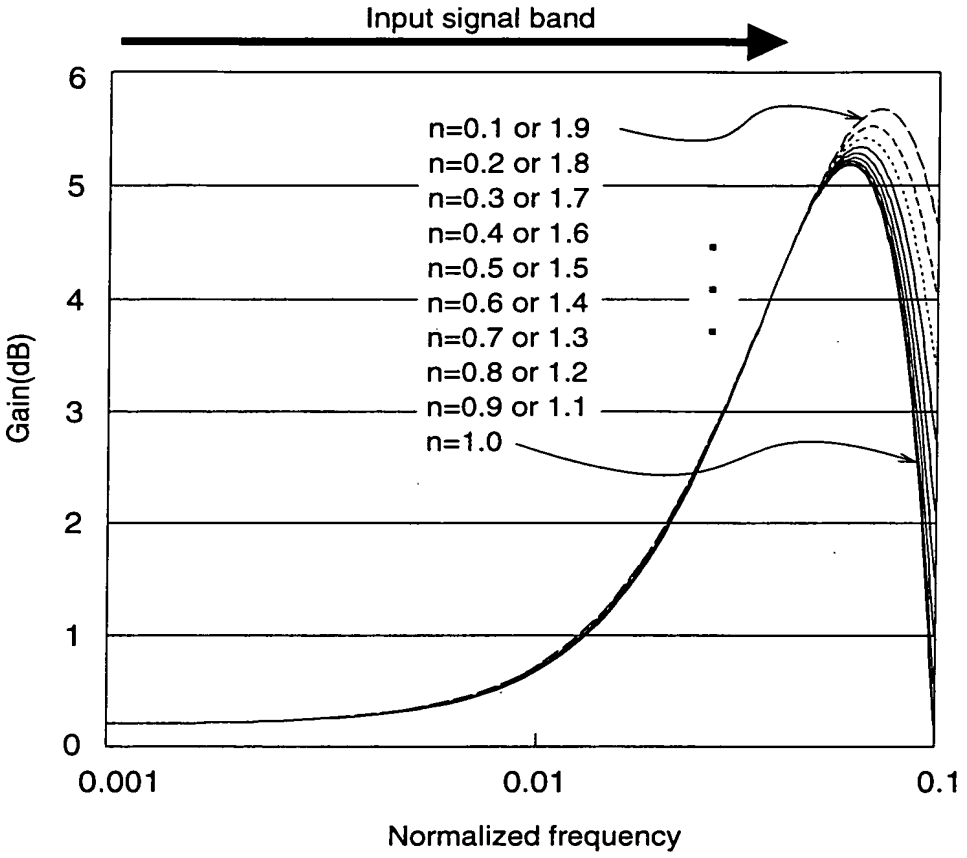

Input signal band
6
5
4
3
2
1
0
Gain(dB)
n=0.1 or 1.9
n=0.2 or 1.8
n=0.3 or 1.7
n=0.4 or 1.6
n=0.5 or 1.5
n=0.6 or 1.4
n=0.7 or 1.3
n=0.8 or 1.2
n=0.9 or 1.1
n=1.0
0.001
0.01
0.1
Normalized frequency

Fig.5

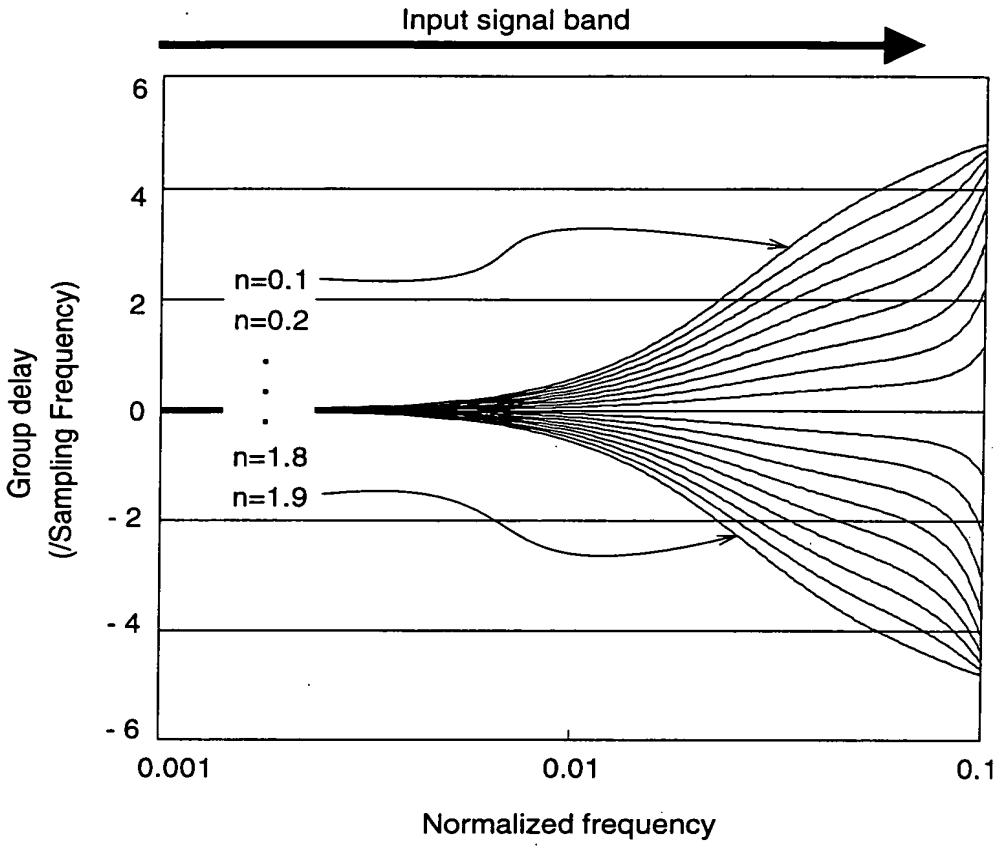

Input signal band
6
4
2
0
- 2
- 4
- 6
n=0.1
n=0.2
n=1.8
n=1.9
Group delay
(/Sampling Frequency)
0.001
0.01
0.1
Normalized frequency

Fig.6(a)

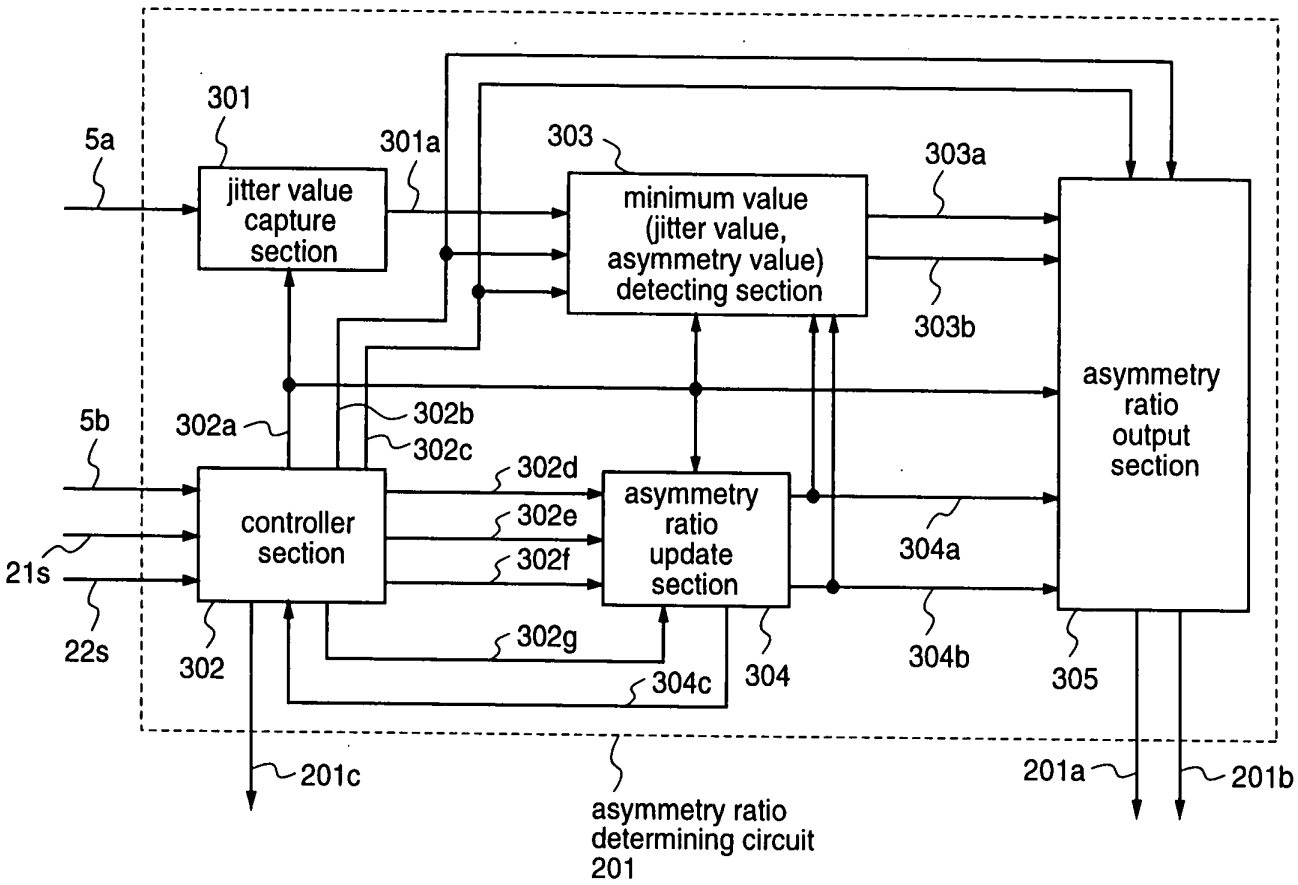

301
5a
301a
303
303a
jitter value capture section
minimum value (jitter value, asymmetry value) detecting section
303b
asymmetry ratio output section
5b
302a
302b
302c
302d
302e
302f
controller section
asymmetry ratio update section
304a
21s
22s
302
302g
304c
304
304b
305
201c
asymmetry ratio determining circuit 201
201a
201b

Fig.6(b)

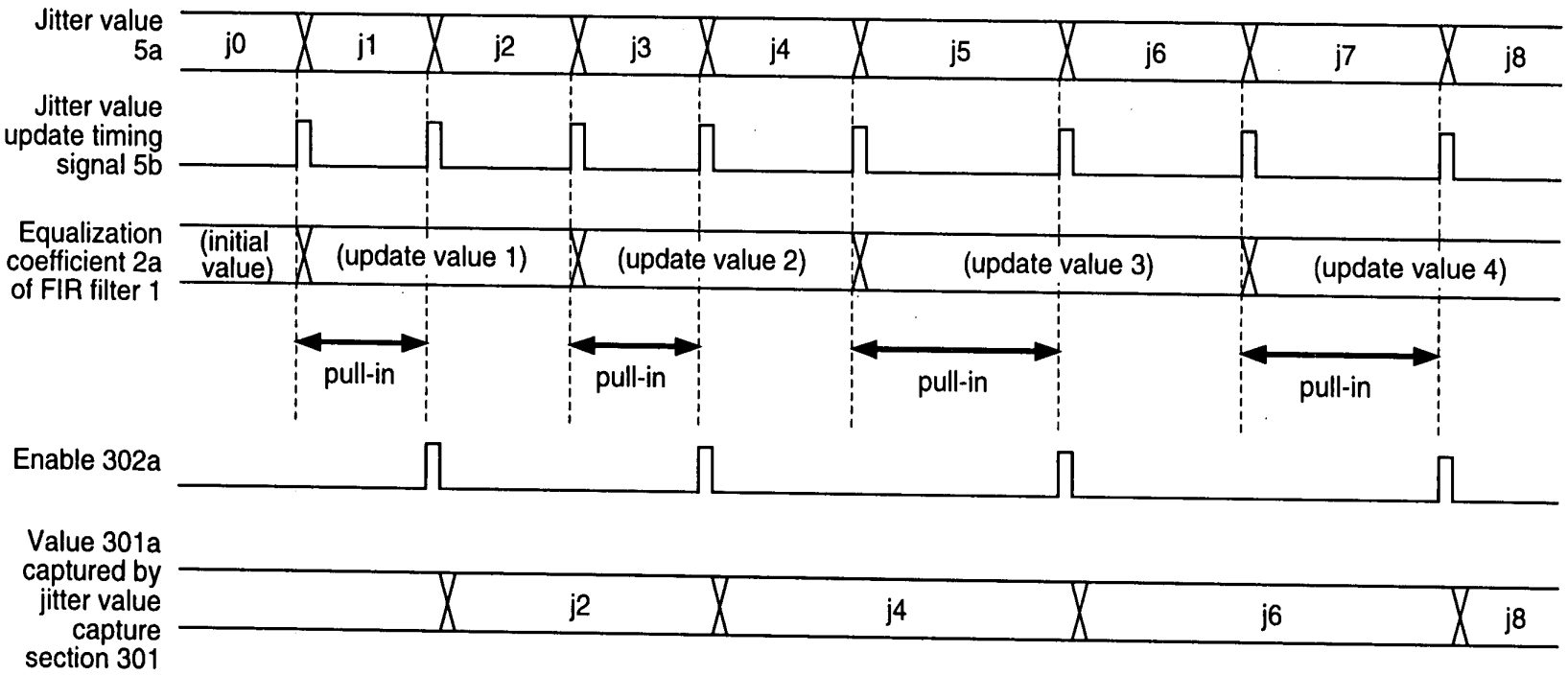

Jitter value 5a
j0
j1
j2
j3
j4
j5
j6
j7
j8
Jitter value update timing signal 5b
Equalization coefficient 2a of FIR filter 1
(initial value)
(update value 1)
(update value 2)
(update value 3)
(update value 4)
pull-in
pull-in
pull-in
pull-in
Enable 302a
Value 301a captured by jitter value capture section 301
j2
j4
j6
j8

Fig.7

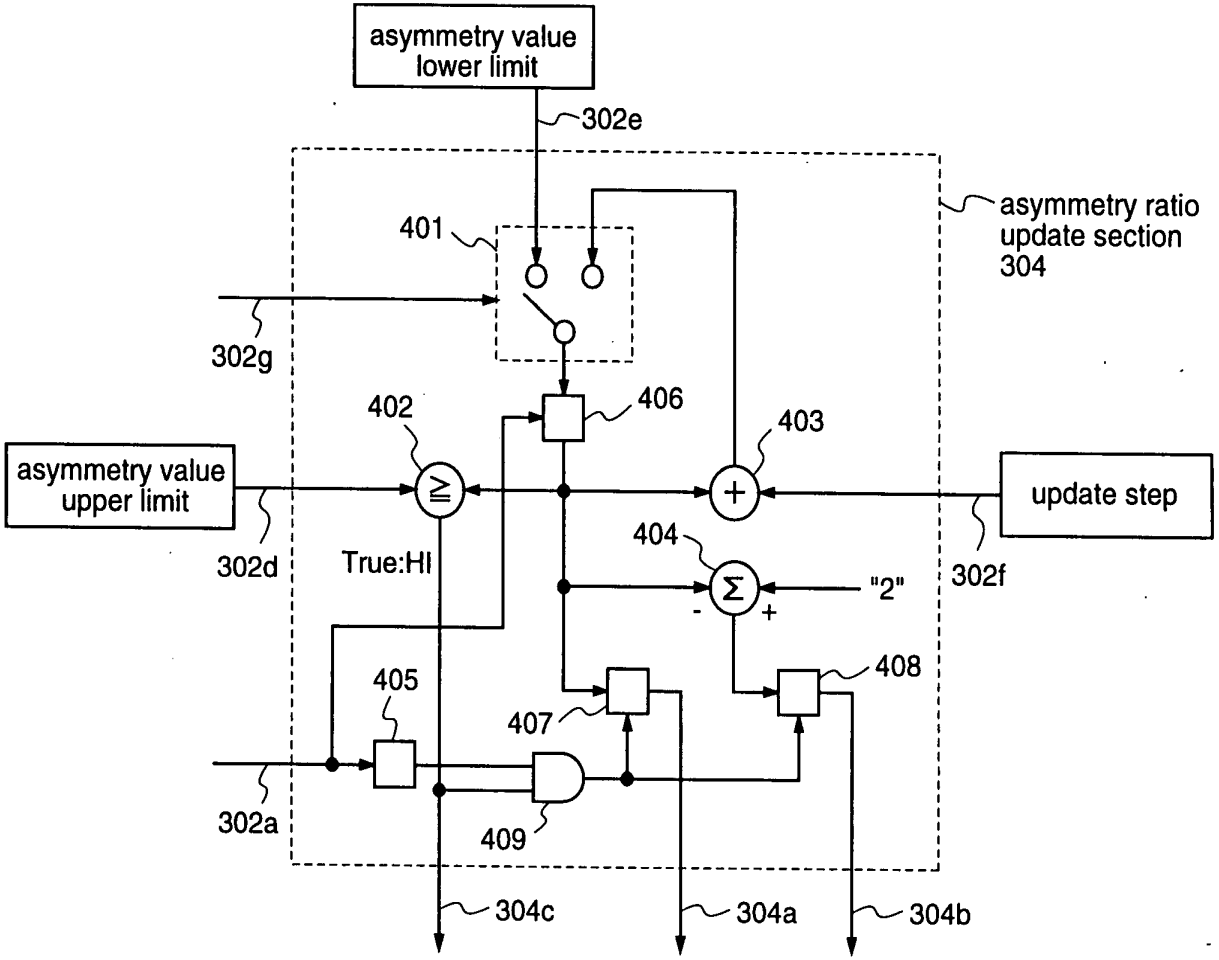

asymmetry value lower limit
302e
asymmetry ratio update section 304
401
302g
402
406
403
asymmetry value upper limit
update step
404
True:HI
"2"
302d
302f
405
407
408
302a
409
304c
304a
304b

Fig.8

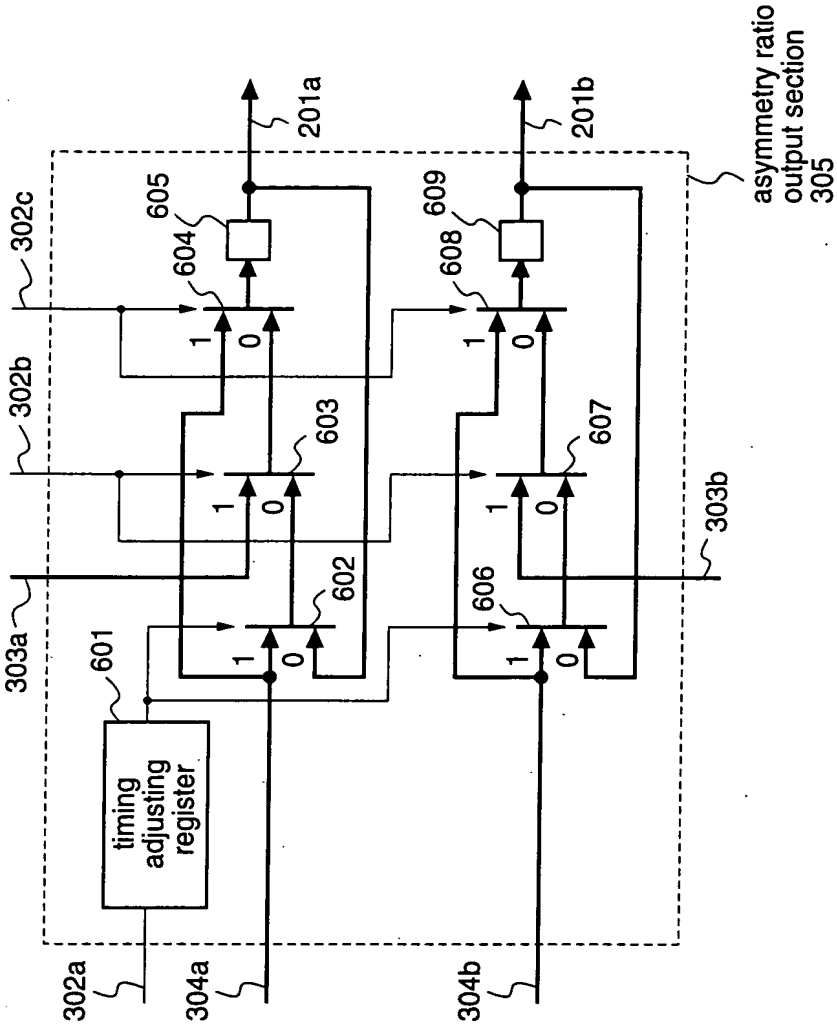

asymmetry ratio output section
305
201a
201b
302c
302b
303a
303b
302a
304a
304b
timing adjusting register
601
602
603
604
605
606
607
608
609
1
0

Fig.9

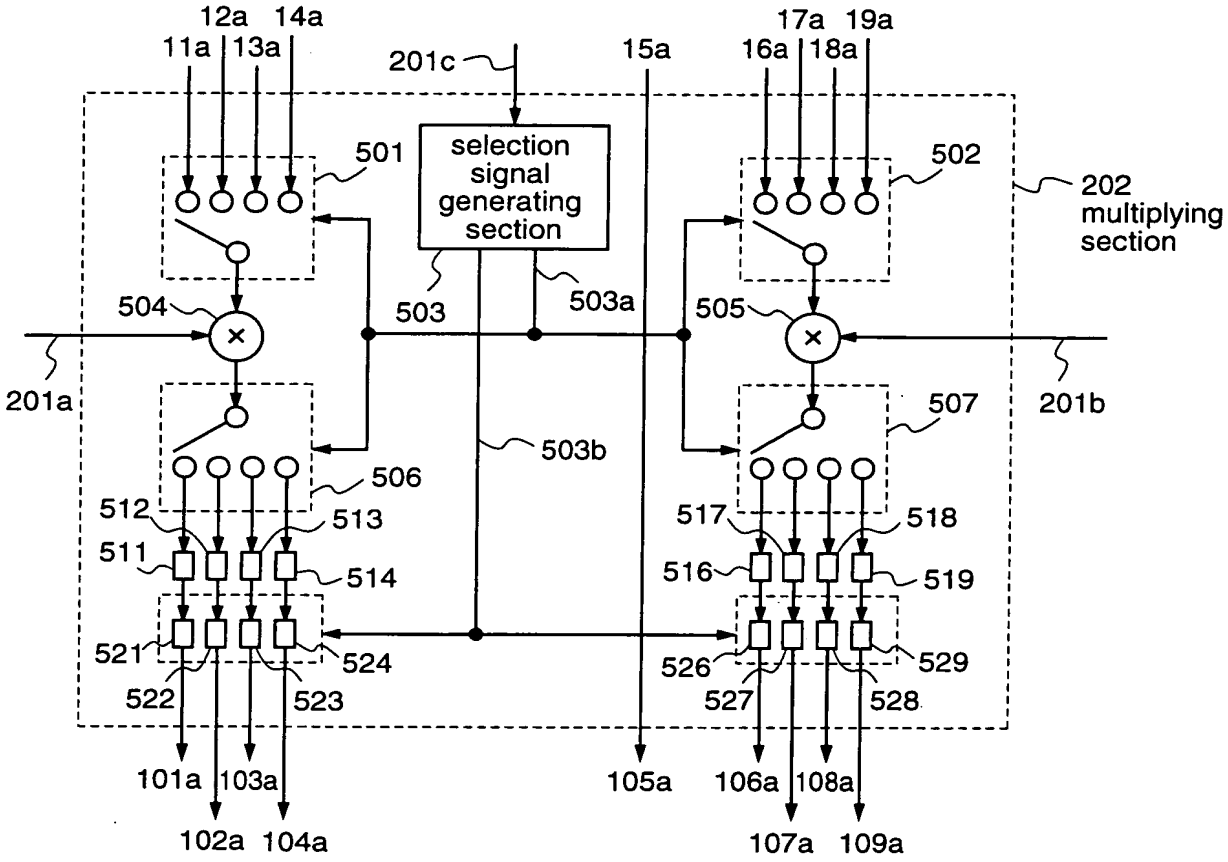

12a
14a
11a
13a
201c
15a
17a
19a
16a
18a
selection signal generating section
501
502
202 multiplying section
504
503
503a
505
201a
201b
503b
507
506
512
513
517
518
511
514
516
519
521
524
526
529
522
523
527
528
101a
103a
105a
106a
108a
102a
104a
107a
109a

Fig.10

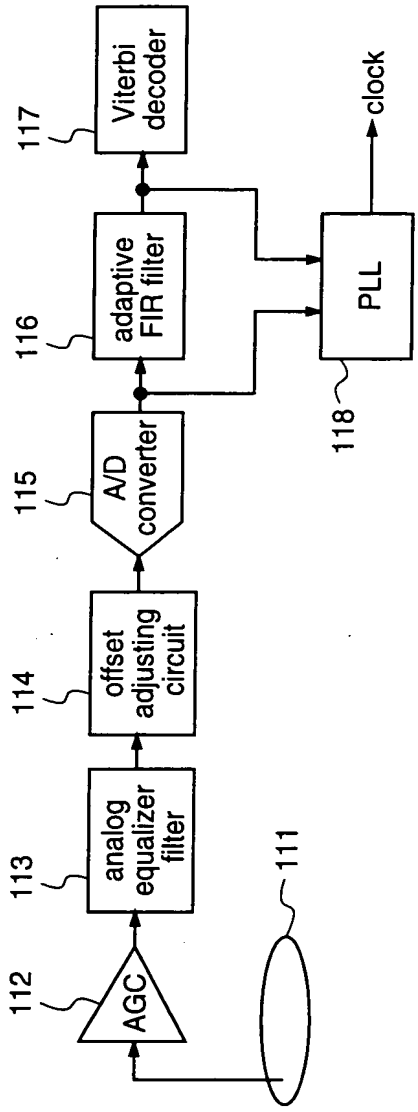
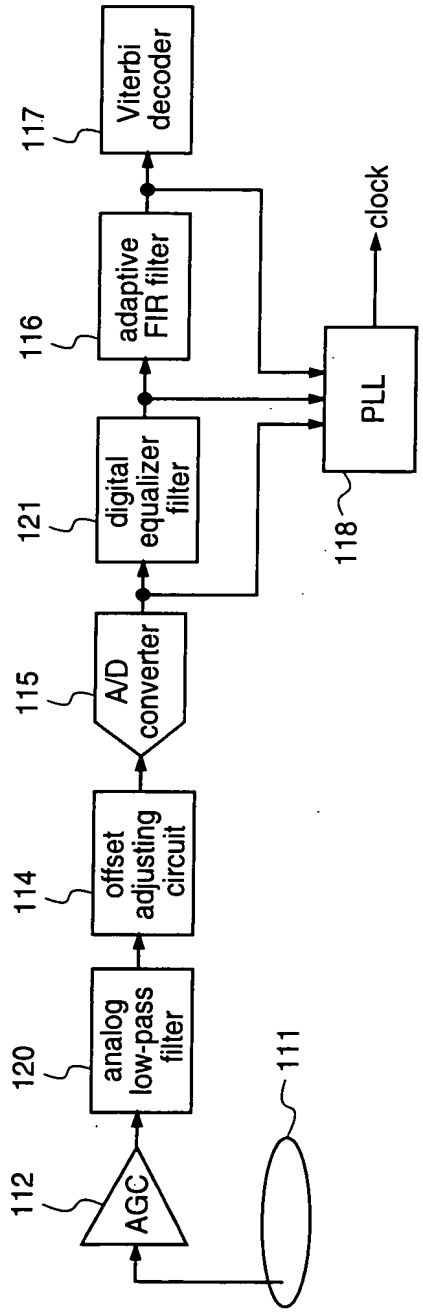

112
AGC
113
analog equalizer filter
114
offset adjusting circuit
115
A/D converter
116
adaptive FIR filter
117
Viterbi decoder
111
118
PLL
clock

Fig.11


112
AGC
120
analog low-pass filter
114
offset adjusting circuit
115
A/D converter
121
digital equalizer filter
116
adaptive FIR filter
117
Viterbi decoder
111
118
PLL
clock